

R07DS0602EJ0100

Rev.1.00

Jan 11, 2012

NP90N055MUK, NP90N055NUK

MOS FIELD EFFECT TRANSISTOR

Description

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Super low on-state resistance
 - $R_{DS(on)} = 3.8 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 45 \text{ A})$
- Low C_{iss} : $C_{iss} = 4900 \text{ pF TYP}$. $(V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing	Package
NP90N055MUK-S18-AY *1	Pure Sn (Tin)	Tube 50 p/tube	TO-220 (MP-25K)
NP90N055NUK-S18-AY *1			TO-262 (MP-25SK)

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 V$)	V _{DSS}	55	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) ($T_c = 25^{\circ}C$)	I _{D(DC)}	±90	A
Drain Current (pulse) *1	I _{D(pulse)}	±360	A
Total Power Dissipation ($T_c = 25^{\circ}C$)	P _{T1}	176	W
Total Power Dissipation ($T_A = 25^{\circ}C$)	P _{T2}	1.8	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to 175	°C
Repetitive Avalanche Current *2	I _{AR}	38	A
Repetitive Avalanche Energy *2	E _{AR}	144	mJ

Notes: *1 $T_C = 25^{\circ}C$, $P_W \le 10 \ \mu$ s, Duty Cycle $\le 1\%$

*2 R_{G} = 25 $\Omega,\,V_{GS}$ = 20 \rightarrow 0 V

Thermal Resistance

Channel to Case Thermal Resistance	R _{th(ch-C)}	0.85	°C/W
Channel to Ambient Thermal Resistance	R _{th(ch-A)}	83.3	°C/W



Electrical Characteristics (T_A = 25°C)

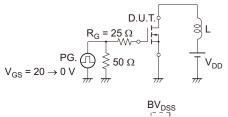
ltem	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions	
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	$V_{DS} = 55 \text{ V}, V_{GS} = 0 \text{ V}$	
Gate Leakage Current	I _{GSS}		_	±100	nA	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$	
Gate to Source Threshold Voltage	V _{GS(th)}	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	
Forward Transfer Admittance *1	y _{fs}	35	70	-	S	$V_{DS} = 5 V, I_{D} = 45 A$	
Drain to Source On-state Resistance *1	R _{DS(on)}		3.15	3.80	mΩ	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 45 \text{ A}$	
Input Capacitance	Ciss		4900	7350	pF	V _{DS} = 25 V	
Output Capacitance	C _{oss}	_	500	750	pF	$V_{GS} = 0 V$	
Reverse Transfer Capacitance	C _{rss}	_	180	330	pF	f = 1 MHz	
Turn-on Delay Time	t _{d(on)}		28	70	ns	$V_{DD} = 28 \text{ V}, I_D = 45 \text{ A}$	
Rise Time	tr		12	30	ns	$V_{GS} = 10 V$	
Turn-off Delay Time	t _{d(off)}		70	140	ns	$R_{G} = 0 \Omega$	
Fall Time	t _f		7	20	ns		
Total Gate Charge	Q _G		80	120	nC	$V_{DD} = 44 V$	
Gate to Source Charge	Q _{GS}	_	21	_	nC	V _{GS} = 10 V	
Gate to Drain Charge	Q _{GD}		20	—	nC	I _D = 90 A	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	$I_F = 90 \text{ A}, V_{GS} = 0 \text{ V}$	
Reverse Recovery Time	t _{rr}		52	—	ns	$I_F = 90 \text{ A}, V_{GS} = 0 \text{ V}$	
Reverse Recovery Charge	Qrr	—	95	—	nC	di/dt = 100 A/µs	

 V_{GS}

0

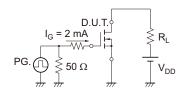
Note: *1 Pulsed test

TEST CIRCUIT 1 AVALANCHE CAPABILITY

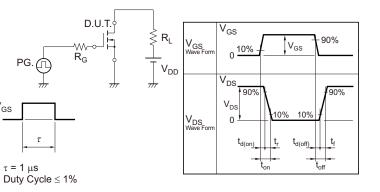


I_{AS} I_{DS} V_{DD} Starting T_{ch}

TEST CIRCUIT 3 GATE CHARGE



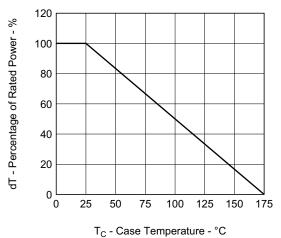
TEST CIRCUIT 2 SWITCHING TIME

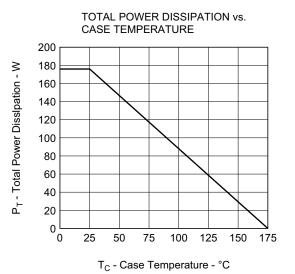




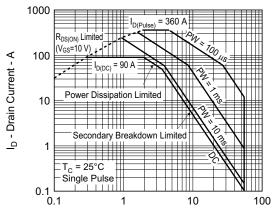
Typical Characteristics $(T_A = 25^{\circ}C)$

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



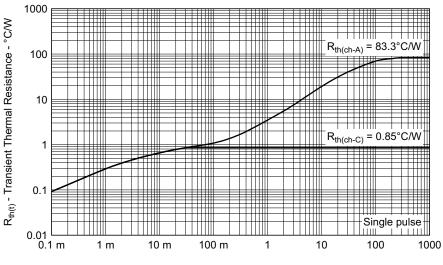


FORWARD BIAS SAFE OPERATING AREA

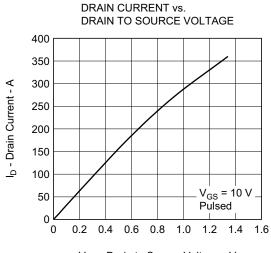




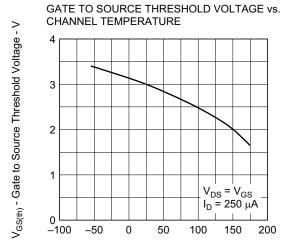
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



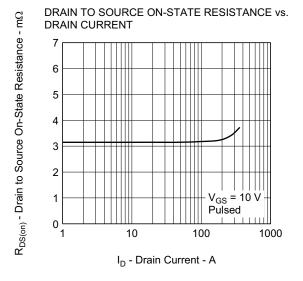




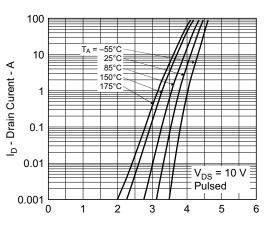
V_{DS} - Drain to Source Voltage - V



T_{ch} - Channel Temperature - °C

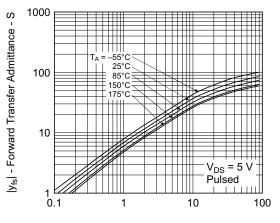


FORWARD TRANSFER CHARACTERISTICS

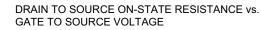


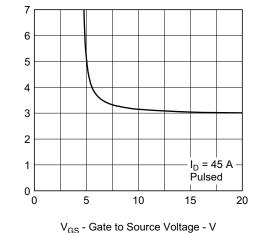


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

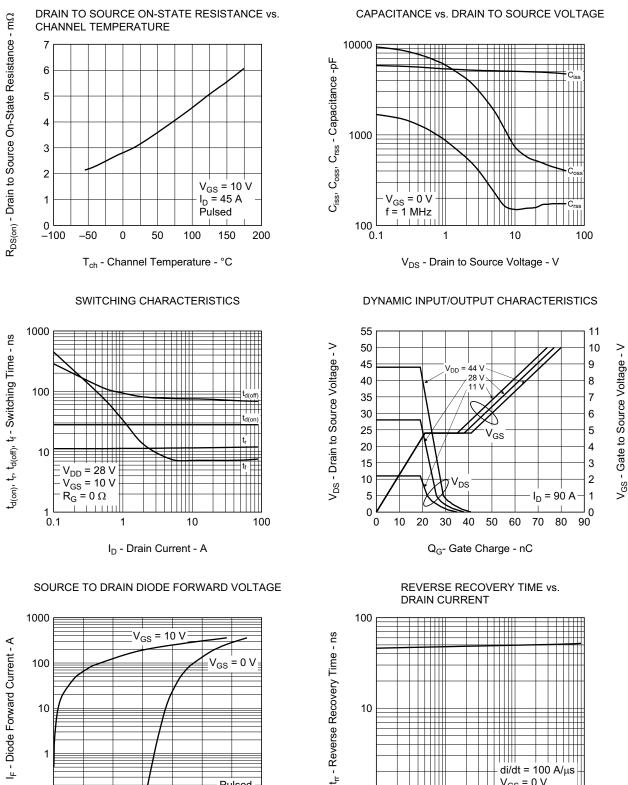


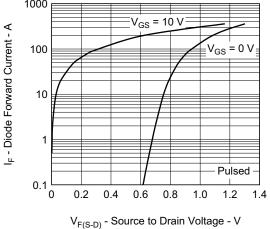
I_D - Drain Current - A





 $R_{DS(on)}$ - Drain to Source On-State Resistance - $m\Omega$







1 └ 0.1

10

IF - Drain Current - A

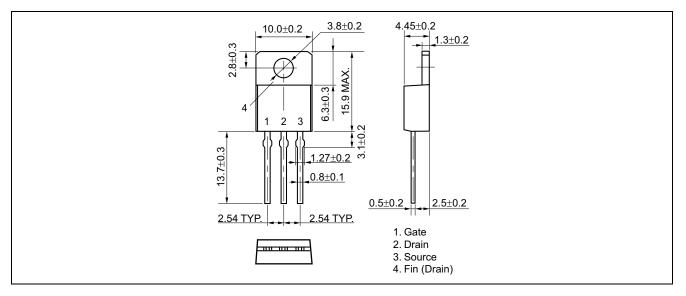
1

di/dt = 100 A/µs $V_{GS} = 0 V$

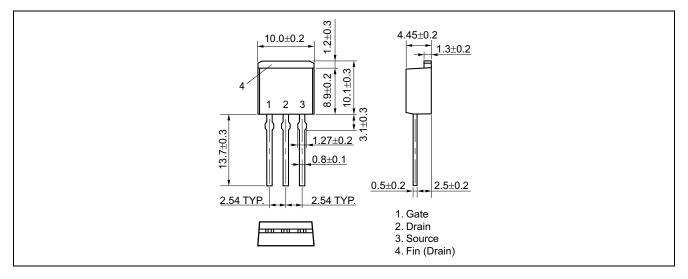
100

Package Drawing (Unit: mm)

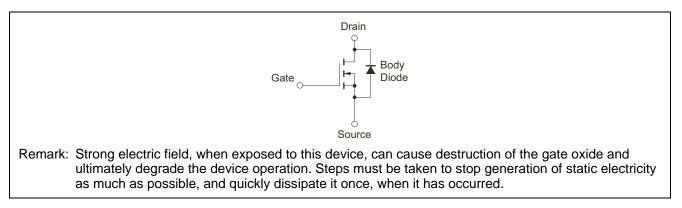
TO-220 (MP-25K) (Mass: 1.9 g TYP.)



TO-262 (MP-25SK) (Mass: 1.8 g TYP.)



Equivalent Circuit





Revision History

NP90N055MUK, NP90N055NUK Data Sheet

		Description			
Rev.	Date	Page	Summary		
1.00	Jan 11, 2012	—	First Edition Issued		

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